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Carbon mediated reduction of silicon dioxide and growth of copper silicide particles in uniform width channels

Filippo Pizzocchero,[a] Peter Bøggild, and Timothy J. Booth
DTU Nanotech, Technical University of Denmark, Ørsteds Plads 344, 2800 Kgs. Lyngby, Denmark

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We show that surface arc-discharge deposited carbon plays a critical intermediary role in the breakdown of thermally grown oxide diffusion barriers of 90 nm on a silicon wafer at 1035 °C in an Ar/H_2 atmosphere, resulting in the formation of epitaxial copper silicide particles in ≈10 μm wide channels, which are aligned with the intersections of the (100) surface of the wafer and the {110} planes on an oxidized silicon wafer, as well as endotaxial copper silicide nanoparticles within the wafer bulk. We apply energy dispersive x-ray spectroscopy, in combination with scanning and transmission electron microscopy of focused ion beam fabricated lammelas and trenches in the structure to elucidate the process of their formation. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4821337]

INTRODUCTION

Metal silicides are of importance in microelectronics and under study currently due to their potential applications in Ohmic contacts, interconnects, gates, diffusion barriers, and due to their determining influence on the properties of the metal/silicon interface.[1] Amongst their favorable properties are high conductivity, thermal stability, and highly tunable growth and synthesis via epitaxial and endotaxial growth or alternative means, depending on the metal and growth substrate in question.[2,3] Also, chemical vapor deposition (CVD) of carbon-containing precursor gases on catalytic metal foils and physically deposited films has recently become a promising route for the scalable growth of graphene, and remains an important tool for the synthesis of other materials on metal catalyst precursors.[4] In general, it is desirable that the catalyst layer for CVD growth is supported by a standard size of silicon substrate, as this ensures compatibility with subsequent microfabrication processing steps and gives the possibility of integrating the as-grown CVD material into a final device without the requirement for physical transfer to another substrate, e.g., by chemical removal of the catalyst layer. It is well known, however, that Cu and Si will form a eutectic at temperatures as low as 800 °C, depending on the ratio of Cu and Si, with the Cu easily penetrating any native oxide through the atomic substitution mechanism.[5] Eutectic formation is also possible in the case of thicker thermally grown silicon oxide diffusion barriers, in the event of pinholes or other defects present in the oxide. However, the exact mechanisms of the formation of copper silicides are not yet well described, leading to some contradictory reports in the literature,[6,7] as has been discussed previously.[8]

Here we present the previously undescribed phenomenon of the formation of relatively ordered and uniform etched channels containing copper silicide particles in the range 1–100 μm in the thermal oxide layer of silicon wafers (Figures 1(a) and 1(b)). Channels with a uniform width of 10 μm, which are exactly oriented along the intersections of the (100) surface of the wafer and the {110} planes occur on a Cu (400 nm)/SiO_2 (90 nm)/Si (350 μm) substrate (Figure 1(c)) only in the presence of a layer of ≈10 nm of arc-discharge deposited carbon at temperatures of 1035 °C in an Ar/H_2 atmosphere. The copper diffusion into the silicon at high temperatures is enhanced by catalytic reduction of the silicon oxide layer in the presence of carbon. During cooling, copper silicide precipitates out of the silicon at the surface forming hemispherical particles, and additionally forms endotaxial copper silicide particles distributed along {110} planes in the interior of the wafer. In the absence of a surface carbon layer, copper instead dewets from the surface of the silicon, and no copper silicide formation is observed.

EXPERIMENTAL SESSION

A thermal oxide layer of 90 nm is grown on undoped 350 μm Si(100) wafers via dry oxidation of Si. A 400 nm thick copper film is deposited via electron beam evaporation (Alcatel E-beam evaporator, 20 $Å s^{-1}$). Subsequent to this, the wafers are exposed to atmosphere before deposition of a ≈10 nm layer of amorphous carbon by arc discharge (Cressington 208HR, 30 s, 4 V, 80 mA.) As a control, we used a physical mask in some cases to selectively inhibit carbon deposition. The samples are then annealed in a CVD furnace used for the growth of graphene (Aixtron Black Magic 4″) at 1035 °C, at a controlled pressure of 10 millibars under a flow of H_2 (100 sccm) and Ar (500 sccm). The substrate temperature is controlled by a thermocouple, with heat supplied by a graphite heater directly in contact with the substrate. Samples were heated up at a rate of 200 $°Cs^{-1}$ to the target temperature, and either held at 1035 °C for 1 min (long anneal) or were heated instantaneously up to 1035 °C (short anneal) before cooling to < 100 °C in 45 min under continued gas flow. The sample structure and annealing conditions are equivalent to those used for the annealing of copper substrates prior to CVD growth of graphene. Our control experiments consisted of carrying out the same procedures, but with the following changes: (1) in the partial absence of carbon (through masking of the

[a]Electronic-mail: filippo.pizzocchero@nanotech.dtu.dk

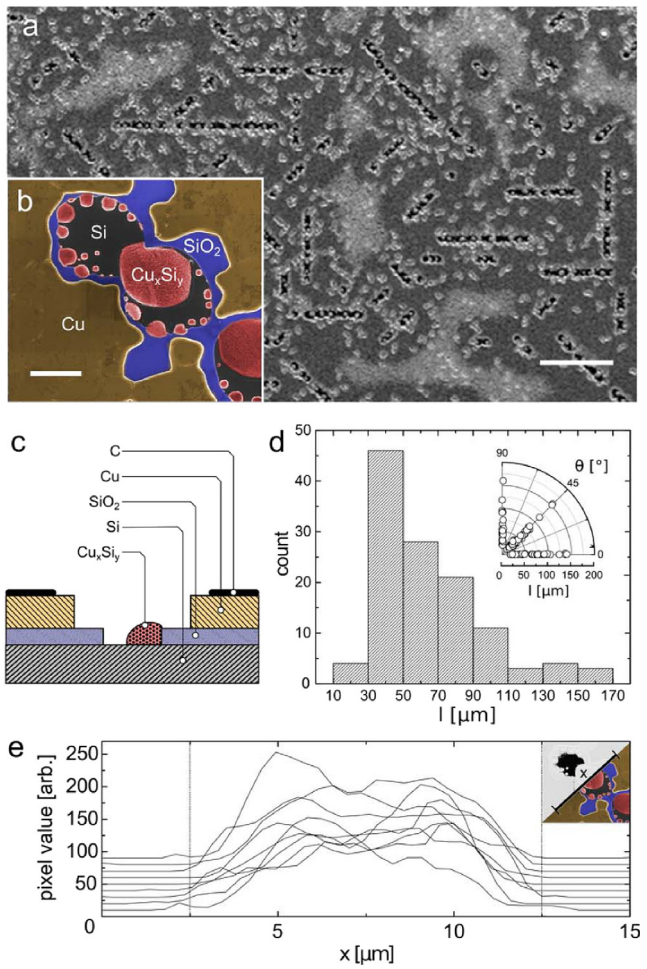

FIG. 1. (a) Channel formation in Cu and SiO_2. Channels are oriented along the intersections of the (100) top surface of the wafer and the {011} planes. Scale 100 μm. (b) Cu dewetting of SiO_2 at edges of channel and copper silicide particle formation in channel. Scale 5 μm. (c) Schematic cross section of sample. (d) Distribution of channel lengths. Inset: polar plot of channel length and orientation. (e) Line profiles for channels in (a). The dotted lines are guides for the eye, spaced 10 μm apart. Inset: Binary thresholding is used to estimate the width of the channel in oxide.

carbon deposition as described above); (2) on silicon wafers with no thermal oxide layer; (3) during vacuum annealing, that is, without the flow of Ar and H_2 described above, and (4) with an instantaneous cooling after the sample reached 1035 °C (short annealing period, as described above).

After annealing, the samples were examined in a FEI Helios NanoLab DualBeam Scanning Electron Microscope (SEM), where lift-out lamellar specimens were produced by Focused Ion Beam (FIB) for investigation of the interior of the sample via SEM and FEI Tecnai G2 Transmission Electron Microscope (TEM). Semiquantitative chemical analyses were performed using Energy Dispersive X-rays Spectroscopy (EDS) in both SEM and TEM and Back Scattered Electron Spectroscopy (BSES) in SEM to provide chemical mapping.

RESULTS AND DISCUSSION

Figures 1(a) and 1(b) present typical results for this procedure. The sputtered copper layer is everywhere penetrated with 10–200 μm long and approximately 10 μm wide striations or channels (Figures 1(d) and 1(e)), which are oriented at 45° with respect to each other and exactly aligned to the intersections of the (100) wafer surface and the {110} planes (Figure 1(d), inset). Figure 1(b) shows the details of one channel, where the copper is seen to dewet the edge of the silicon oxide channels, which in turn contain a number of particles. The channels present quite irregular edges, with a line roughness on the order of 5 μm in the Cu layer, and 1 μm in the underlying oxide layer (Figure 1(e)). The particles inside the channels exhibit roughness on the nanometer scale that qualitatively appears to increase with particle size; this tendency was present in all the data.

EDS and BSES results showing the relative presence of copper, silicon, and oxygen are presented in Figures 2(a)–2(d). Copper is detected in the x-ray spectrum around the channel and to a lesser extent also in the particles within the channel. The spectral maps indicate an increased presence of silicon in the opening in the copper, with a stronger silicon response from the inner channel, indicating that the inner channel consists mainly of exposed silicon. Oxygen is most abundant between the outer and inner channels, indicating silicon oxide is still present in these regions, and on the areas of the particles where copper is less abundant, possibly indicating silicon oxide is present on the surface of the particles as well. It is not possible to resolve the presence of carbon using SEM-EDS in our experiments due to the low atomic number of carbon. Secondary electron imaging, however, shows lighter contrast in areas away from channels, which may indicate depletion of the deposited surface carbon around channels (Figure 2(e)). Quantitative analysis is hampered by the complex and heterogeneous 3D structure of the sample making the precise boundary of the x-ray interaction volume indeterminate.

To probe the 3D structure of the sample, a lamellar section across a channel was prepared using FIB, directly through a particle in a channel, for study in the TEM. A bright-field TEM montage micrograph is shown in Figure 2(f). Prior to definition of the lamella and the subsequent liftout, a Pt capping layer is deposited *in-situ* by FIB deposition on the surface for protection during preparation and for bonding to the liftout probe; this layer is labeled in Figure 2(f). The deposited copper, thermal oxide, silicon substrate and surface, and endotaxial copper silicide particles are also labeled. Endotaxial copper silicide deposits are visible arranged along the cross section of the (110) plane: the size of these deposits is qualitatively seen to reduce further from the substrate surface (i.e., deeper in the wafer). EDS spectra acquired *in-situ* in the TEM are shown in Figures 2(g)–2(j), with Figure 2(f) indicating the region from which the spectrum was acquired. A weak response corresponding to the carbon K edge is visible in TEM EDS in Figure 2(h) around 0.3 keV in the bulk silicon. Both the endotaxial and surface silicide particles (Figures 2(i) and 2(j)) are rich in both copper and silicon, with potentially some oxygen present in the surface particle (Figure 2(j)) – a 2–3 μm thick layer of silicon oxide is also visible under the surface particle (Figure 2(f)).

In the cross-sectional image presented in Figure 2(f) the hemispherical top surface of the particle contrasts starkly with the lower boundary of the particle, which shows a complex fractal-like interface with the silicon oxide beneath it.

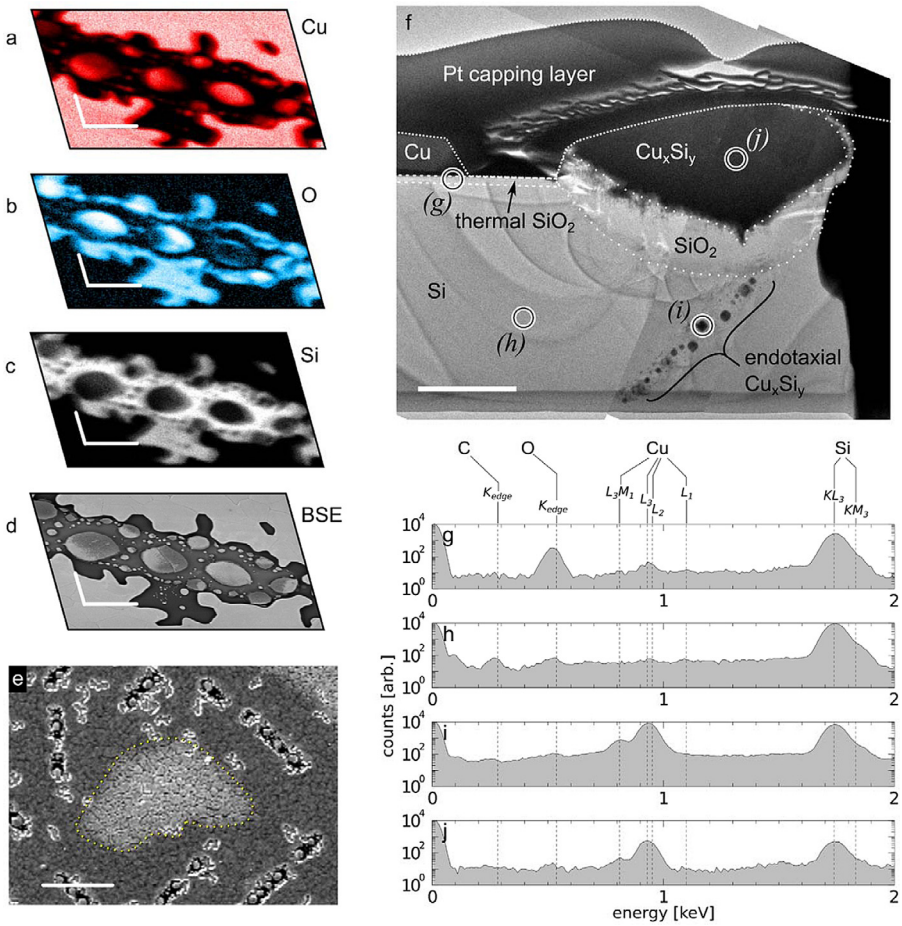

FIG. 2. (a)–(c) EDS mapping of elemental abundance of Cu, O, Si. Abundance is indicated by pixel gray value. Scale bars 10 μm. (d) Backscattered electron detector image of corresponding area. Scale bar 10 μm. (e) Light contrasting regions between channels, marked by dotted boundary could indicate the presence of carbon, which is not detectable via SEM EDS in our experiments. Scale bar 50 μm. (f) TEM image (montage) of a lamellar cross section through a particle. Pt capping layer used during sample preparation is marked. Also visible is a copper silicide particle at the surface with an underlying silicon oxide layer with fractal boundary; and smaller endotaxial copper silicide particles gathered on a (011) plane. Rings with italic labels indicate regions where EDS spectra are taken. Scale bar 5 μm. (g)-(j) EDS spectra from the indicated regions in (f). Principal edges and transition energies are marked for C, O, Cu and Si. Spectra qualitatively indicate a higher relative abundance of Cu in the endotaxial particles (i) and emerging particle (j), and of C in the bulk (h). O is measured most strongly in the oxide layer (g).

By partially shadow-masking the surface (see Experimental Section), regions with and without carbon deposition are defined. In areas protected from carbon deposition there is a complete absence of channels, and instead we observe a dewetting of the copper from the oxide layer, with voids of around 10 μm opening on the surface. In areas outside the masked region carbon deposition led to the expected channeling behavior as observed previously. The transition area between these areas is less than 5 μm at the edge of the shadow mask (Figure 3(c)).

In the absence of a thermal oxide layer, the same experiment leads to the strong formation of silicides universally over the surface, as expected from previous reports.[9] In the absence of gases during the annealing step, i.e., under a vacuum of 10^{-3} millibars, the channels do not form, and the copper does not dewet from the surface. The experiment was also carried out at reduced temperatures of 800–1000 °C with no evidence of channels observed.

Figures 3(d) and 3(e) shows the results of the process where the sample is only allowed to heat up to 1035 °C instantaneously before being cooled. In this case, the precipitation of surface silicide particles partially delaminates the deposited copper from the surface. A cross section through a particle using FIB shows the copper delaminating from the oxide (Figure 3(e)).

It is well known that copper forms a eutectic with silicon, with the eutectic melting temperature occurring around 800 °C, as compared to 1083 °C for pure copper.[10] Copper deposited on an oxidized silicon wafer with an oxide layer thick enough to suppress the substitutional movement of copper atoms through the oxide and into the bulk will show dewetting at temperatures approaching the melting temperature of copper. In this work we observe that this dewetting can be suppressed in the presence of an evaporated layer of carbon (Figure 3(c)). Although the mechanism for this is not clear, possible reasons for the difference observed include (1) that the evaporated carbon reduces the surface energy of the copper-atmosphere interface; or alternatively (2) the carbon prevents the evaporation of copper at high temperature.

A perfect oxide layer should form an effective barrier against diffusion of copper into the bulk silicon;[11,12] however, in this work we observe the formation of particles of copper silicide in areas where carbon is present, and a lack of silicide formation where carbon is absent. This leads us to the conclusion that the carbon is playing a key role in the penetration of the oxide layer (Figure 3(a-i,ii)). The reduction of silicon oxide by carbon at high temperatures has been reported previously, through the formation of a silicon carbide intermediate.[13] It is likely then that carbon comes into contact with the silicon oxide through diffusion between copper grains (the area density of grain boundaries would then determine the area density of channels formed) or in pinholes in the copper film whilst the copper is more mobile at elevated temperature. The carbon then reduces the silicon oxide, forming sites where copper is able to penetrate the oxide more easily (Figure 3(a-iii)).

It is known that the particles form during the cooling of the substrate, with the copper silicide eutectic precipitating out of the Si at faults or voids in the crystal structure, and then at the exposed surface of the substrate (Figure 3(a-iv,v)).[7,8,14]

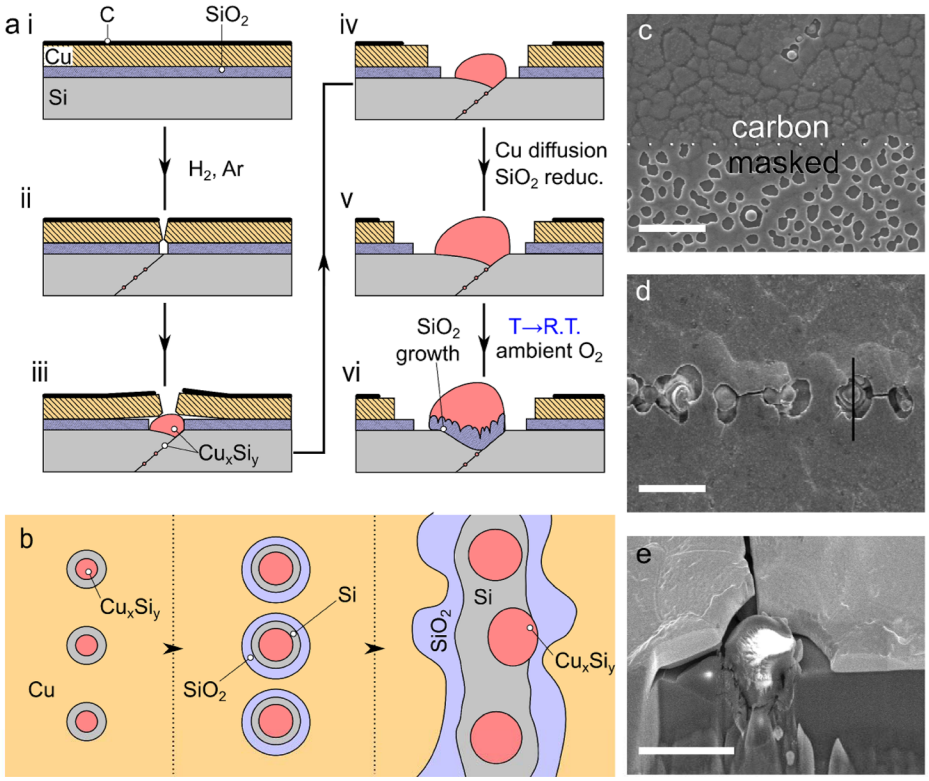

FIG. 3. (a) Schematic of the formation of CuSi particles. (i) The initial state of the sample. (ii) During annealing, the copper forms grains. Sputtered carbon on the surface is then allowed to come into contact with the oxide layer by diffusion through grain boundaries. The oxide layer is removed through carbothermal reduction, and copper diffuses into the bulk silicon. (iii)–(iv) Cooling the sample results in precipitation of copper silicide particles beneath the copper layer, which delaminates the copper, as seen in Figures 3(d) and 3(e). Reduction of silicon dioxide by carbon results in breakdown of the oxide diffusion barrier, and allows copper to diffuse into the silicon. (v) Continued annealing results in a higher concentration of copper in the silicon. (vi) On exposure to ambient atmosphere, the CuSi particles catalyse the formation of silicon oxide at the CuSi/Si interface (c.f. Figures 2(b) and 2(f)). (b) Schematic plan view of channel formation. Initially emerging particles grow at a uniform rate, removing the surrounding copper and oxide layers until the removed areas join into a channel with a relatively uniform width. (c) Masked deposition of carbon results in dewetting of copper from silicon oxide in the masked region. (d) SEM micrograph of particles emerging from the surface of the substrate. (e) SEM micrograph of FIB cross sectional view of silicide particle emerging from the substrate.

The faults in the crystal are probably intrinsic,[15] and the copper silicides initially precipitate there. There is substantial stress in the Si lamella investigated, visible from the presence of bend contours in the crystal (Figure 2(f)). This is caused by compressive stress induced by this precipitation, and expected since $a_{Si} < a_{CuSi}$.

Our interpretation of the highly uniform width of the channels is that the emerging silicide particles gather along the edge of the intersections of the (100) wafer surface and the {110} planes, and continue to catalytically remove the silicon oxide and grow by absorption of surface copper, at a rate determined by the prefactor and activation energy for the catalytic removal of silicon oxide. The width of the channels in the copper would then be determined by the width of the channel in the silicon dioxide, but widened and roughened somewhat from the local dewetting and consumption of the copper during silicide particle formation and growth. We therefore ascribe the striking uniformity in average width of the inner channels etched in the silicon oxide to the uniform rate of reduction of silicon oxide by copper silicide over the wafer surface as previously observed.[16] Copper silicide is known to catalyse the reverse reaction of oxidation of silicon to silicon oxide even at room temperature[17]—a process which we believe explains our observation of an indistinct 2–3 μm layer of silicon oxide with a fractal boundary beneath the particle visible in Figure 2(f), similar to previous reports.[18]

CONCLUSIONS

We have presented results on the annealing of copper in a reducing environment on thermally oxidised silicon wafers, in the presence of a carbon surface layer. The carbon supresses the dewetting of the copper on silicon dioxide, and at temperatures of 1035 °C reduces the 90 nm oxide layer, allowing subsequent copper substitution into the silicon wafer and the formation of copper silicide eutectics. During heating, or on cooling, 1–10 μm diameter copper silicide particles are precipitated at the intersection of the (100) surface of the substrate and the {011} planes, with silicide particles of $< 1\,\mu$m diameter visible along {011} planes in the bulk of the substrate, introducing substantial strain. At the substrate surface, channels with highly uniform widths of around 10 μm are produced in both the oxide and the copper surface layer that are exactly oriented with the intersection of the (100) surface of the substrate and the {011} planes.

The role of carbon in the suppression of dewetting of copper on silicon oxide has implications for the catalytic growth of carbon nanomaterials on silicon-supported copper catalysts where silicon dioxide is used as a diffusion barrier, e.g., for the growth of graphene via CVD, and highlights the need for effective oxide barriers in the presence of reducing environments and carbon. The presence of pinholes or other

faults in a barrier oxide will hasten the onset of silicide formation.

The formation of copper silicide eutectics in general and the physics of metal semiconductor interfaces is a subject of current research, and the determining role of carbon in the breakdown of oxide diffusion barriers demonstrated here may have relevance for the semiconductor industry—particularly in the case where copper is used as a via material in 3D packaging. Alternatively, further research on controlling the density and size of the silicide precipitates could result in processes for the controllable formation of patterned high density surface coatings of silicide micro- and nanoparticles for MEMS purposes or subsequent catalytic growth.

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